

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor integrated circuit device comprising:
  - a trench formed in a semiconductor substrate and defining active regions and dummy regions;
  - an element isolation insulating film buried in said trench such that said element isolation insulating film serves as an element isolation region;
  - an interlayer insulating film covering said substrate and said dummy regions and ~~including an~~ comprising a planarized insulating film ~~planarized~~; and
  - external terminals formed over said interlayer insulating film such that said dummy regions are formed under said external terminals.
2. (previously presented) A semiconductor integrated circuit device according to claim 1, wherein a length of said dummy region is shorter than a distance between said external terminals.
3. (canceled)
4. (canceled)
5. (canceled)
6. (previously presented) A semiconductor integrated circuit device comprising:

a trench formed in a semiconductor substrate and defining active regions and dummy regions;

an element isolation insulating film buried in said trench such that said element isolation insulating film serves as an element isolation region;

gate electrodes formed over said active regions and serving as gate electrodes of MISFET type elements; and

dummy patterns each comprised of a same layer as said gate electrodes and formed in a region spaced from said gate electrodes and a marker portion for photolithography.

7. (new) A semiconductor integrated circuit device according to claim 6, wherein said dummy regions are formed at a scribing area.

8. (new) A semiconductor integrated circuit device comprising:

interconnections formed over a semiconductor substrate; and

dummy interconnections each comprised of a same layer as said interconnections and spaced from said interconnections; and  
an insulating film covering said interconnections and said dummy interconnections and comprising a film planarized by polishing,  
wherein said dummy interconnections are formed at a scribing area,  
wherein a length of said dummy interconnection is shorter than a distance between external terminals.

9. (new) A semiconductor integrated circuit device according to claim 8, wherein at least some of said dummy interconnections are formed under said external terminal, and wherein said external terminal is a bonding pad.

10. (new) A semiconductor integrated circuit device according to claim 8, wherein said dummy interconnections are arranged to be spaced from a marker portion for photolithography.

11. (new) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

element isolation insulating films buried in said trenches such that said element isolation insulating films serve as element isolation regions,  
wherein said dummy regions are formed at a scribing area.

12. (new) A semiconductor integrated circuit device according to claim 11, wherein a length of said dummy region is shorter than a distance between external terminals.

13. (new) A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions; and

insulating films buried in said trenches such that said insulating films serve as element isolation insulating films;

wherein said dummy regions are formed at a scribing area.

14. (new) A semiconductor integrated circuit device according to claim 13,  
wherein a length of said dummy region is shorter than a distance between bonding  
pads.

15. (new) A semiconductor integrated circuit device comprising:  
trenches formed in a semiconductor substrate and defining active regions and  
dummy regions; and  
element isolation insulating films buried in said trenches,  
wherein said dummy regions are formed at a scribing area.

16. (new) A semiconductor integrated circuit device according to claim 15,  
wherein a length of said dummy region is shorter than a distance between external  
terminals.